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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,800	11/08/2001	Mark A. Gerber	SC11588TK	7112

23125 7590 04/15/2003

MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
7700 WEST PARMER LANE MD: TX32/PL02
AUSTIN, TX 78729

EXAMINER	
ROMAN, ANGEL	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 04/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,800	GERBER ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 01/24/03 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

2. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4. It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

3. **Correction of Informalities -- 37 CFR 1.85**

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

4. **Corrections other than Informalities Noted by Draftsperson on form PTO-948.**

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3-15, 28 and 29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant's incorporated new limitation to claims 3 and 6, "no substrate is interposed between the first integrated circuit and the second integrated circuit", is not supported by the specifications since there are two substrates (24, 30) interposed between the integrated circuits (22, 32).

7. Claims 4, 5, 7-15, 28 and 29 are rejected for their dependency on rejected claims 3 and 6 respectively.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 6, 7 and 11-15 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shin et al. U.S. Patent 6,515,356 B1.

Shin et al. discloses a method for forming, a package device, comprising; providing a package substrate 10 having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane (see figure 10A); attaching a tape C to the package substrate along the first plane (see figure 10A); placing a first integrated circuit 2 on the tape C and in the cavity (see figure 10C); depositing encapsulating material 20 over the first integrated circuit 2 (see figure 10E); removing the tape C (see figure 10G); placing a second integrated circuit 3 adjacent to the first integrated circuit 2 outside the cavity; and depositing encapsulating material over the second integrated circuit (see figure 6A). The second integrated substrate 3 is placed adjacent to the first integrated substrate 2

outside the cavity, such that no substrate is interposed between the first integrated circuit 2 and the second integrated circuit 3 (see figure 6A). A first portion of the encapsulating material 20 is deposited over the first integrated circuit 2 prior to the step of placing the second integrated circuit 3; and a second portion of encapsulating material is deposited over the second integrated circuit 3. The package substrate further comprises first pads on the first surface, second pads on the second surface, first bond fingers 12 on the first surface, and second bond fingers on the second surface, further comprising; electrically connecting by wire bonding the first integrated circuit to the first pads; and electrically connecting the second integrated circuit to the second pads (see figure 6A). The supporting member C may comprise an electrically conductive material (see column 10, lines 21-27). The step of depositing the first portion of the encapsulating material 20 comprises transfer molding the encapsulating material (see figure 13).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 2-5, 9, 10 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. U.S. Patent 6,515,356 B1 in view of Higgins, III U.S. Patent 5,291,062 A.

Shin et al. is applied as above but lacks anticipation on testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads; and disclosing a transfer molding process for encapsulating the second integrated circuit.

With respect to testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads, Higgins, III discloses testing an integrated circuit by applying test probes (see column 4, lines 32-40). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the integrated circuit in the primary reference of Shin et al. by applying probes as disclosed in Higgins, III, since unnecessary packaging cost may be prevented by testing the circuit functionality.

Regarding disclosing a transfer molding process for encapsulating the second integrated circuit, it would have been obvious to a person having ordinary skills in the art

at the time the invention was made to disclose a transfer molding process for the second integrated circuit 3 in the primary reference of Shin et al. since Shin et al. is already using a transfer molding process for the first integrated circuit.

13. Claims 8 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. U.S. Patent 6,515,356 B1 in view of Higgins, III U.S. Patent 5,291,062 A as applied to claims 2-5, 9, 10 and 28 above, and further in view of Halahan U.S. Patent Application Publication 2003/0047798 A1.

Shin et al. as modified by Higgins, III is applied as above but lacks anticipation on disclosing a third integrated circuit adjacent to the second integrated circuit prior to the step of depositing the second portion of encapsulating material, wherein the third integrated circuit is stacked at least partially overlying one of the first and second integrated circuits. Halahan discloses stacking a third integrated circuit 104.2 adjacent to a second integrated circuit, wherein the third integrated circuit is stacked at least partially overlying one of a first and second integrated circuits (see figure 1). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a third integrated circuit adjacent to the second integrated circuit prior to the step of depositing the second portion of encapsulating material, wherein the third integrated circuit is stacked at least partially overlying one of the first and second integrated circuits in the primary reference of Shin et al. as modified by Higgins, III as disclosed in Halahan since it would provide a desire package density.

Response to Arguments

14. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Vaiyapuri, Komiyama and Shimada disclose methods of forming packaging devices comprising; providing package substrates having a first surface along a first plane and providing second surface along a second plane, wherein the package substrates have a cavity between the first plane and the second plane; placing a first integrated circuit in the cavity; placing a second integrated circuit adjacent to the first integrated circuits outside the cavity, such that no substrate is interposed between the second integrated circuit and the first integrated circuit; and depositing encapsulating material over the first integrated circuit and the second integrated circuit. Van Campenhout discloses a method of forming a packaging device by stacking plural integrated circuits

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
April 9, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800